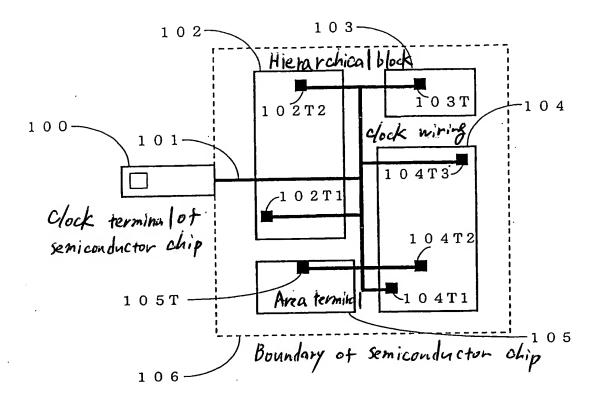
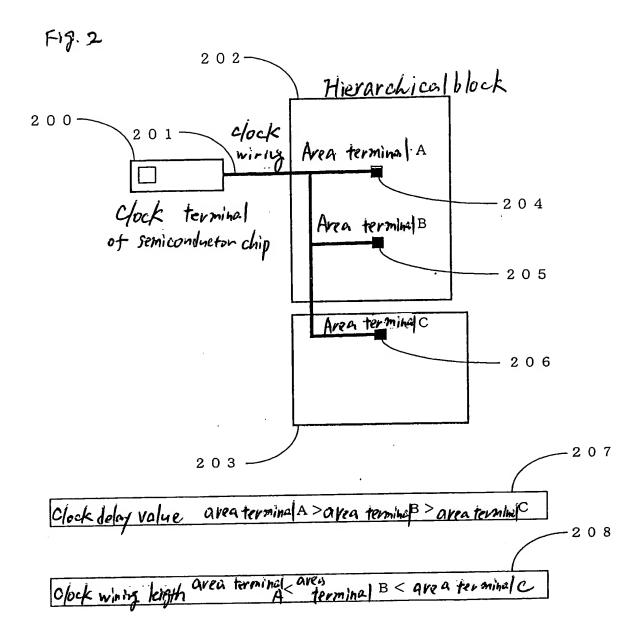
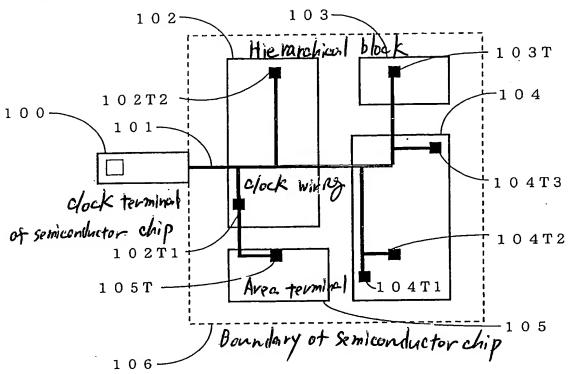
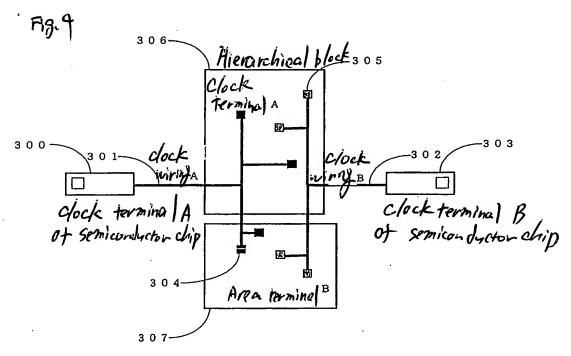
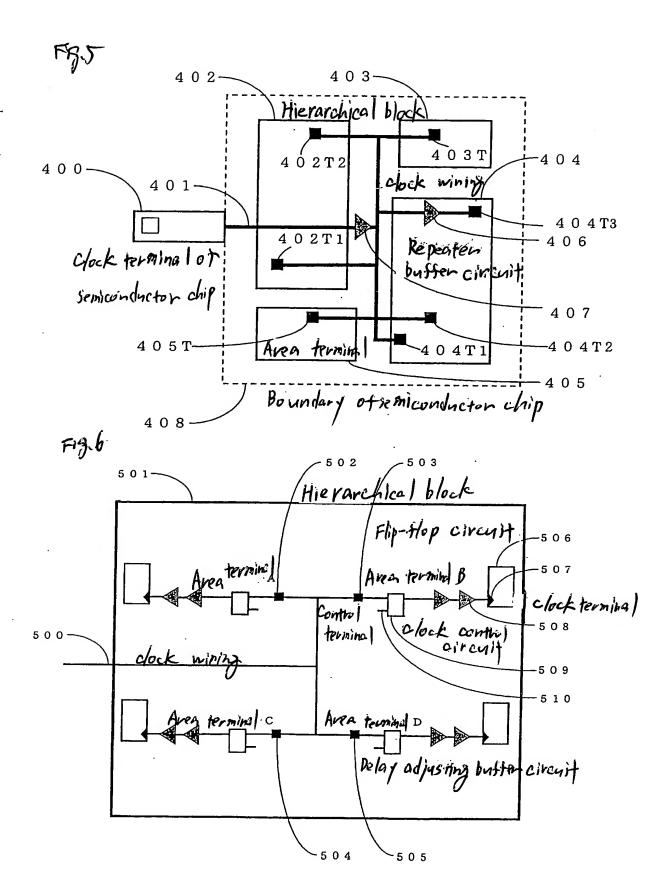
Fig.

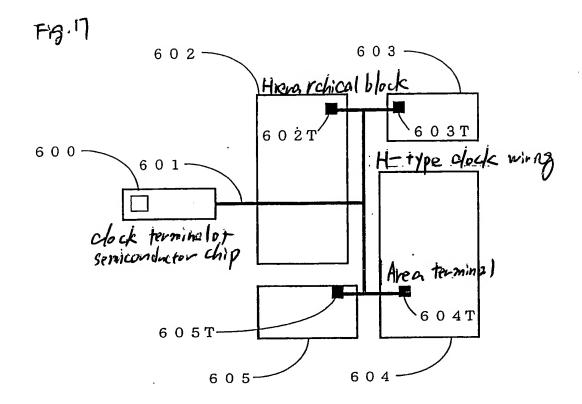


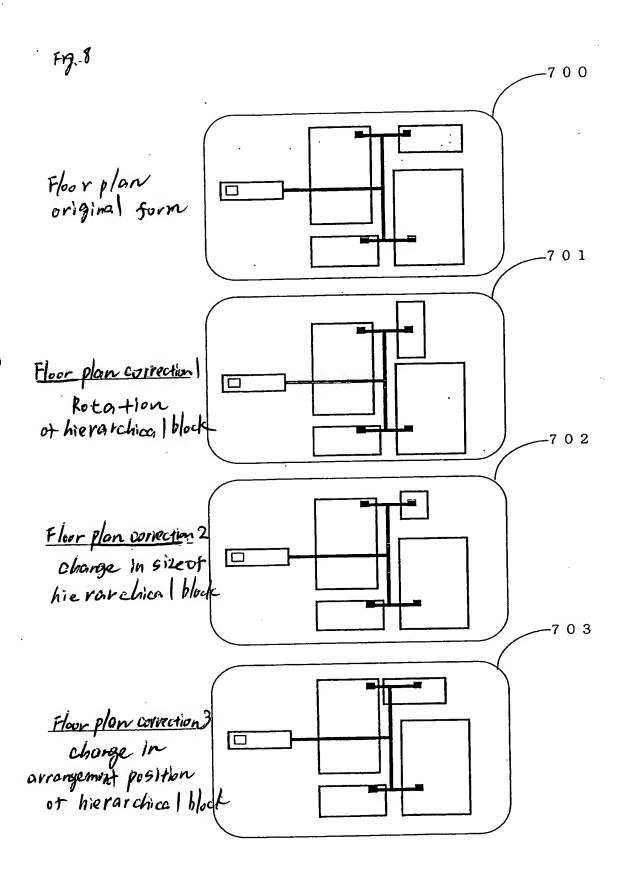












Execute CTS every area terminal of each
hierarchical block and make a clock delay value unitorm

8 0 1

between the adjustment of a clock delay between the hierarchical blocks of one chip through an equal-length wiring from the clock terminal of a semiconductor Chip to the area terminal of each hierarchical block

8 0 2

Generate a place in which a clock delay value from the area terminal of a certain hierarchical block to the CK terminal of each FF does not satisfy a Synchrohous desired value

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Execute the CTS in the area terminal of the hierarchia) block to be an object again, thereby seting a clock deby value to be a desired value.

